Electrical and Computer Engineering

ECE 462  Logic Synthesis  credit: 3 hours.
Unate function theory, unate recursive paradigm, synthesis of two-level logic, synthesis of incompletely specified combinational logic, multi-level logic synthesis, binary decision diagrams, finite state machine synthesis, automatic test pattern generation and design for test, equivalence checking and reachability analysis of finite machines, and technology mapping. 3 undergraduate hours. 3 graduate hours. Prerequisite: ECE 220 or CS 233.

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<th>CRN</th>
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<td>33957</td>
<td>Discussion/Recitation</td>
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<td>11:00 AM - 12:20 PM</td>
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<td>3081 - Electrical &amp; Computer Eng Bldg</td>
<td>Huang, T</td>
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Credit Hours: 3 hours